# DG458/459

## Fault Protected Single 8-Ch/Differential 4-Ch Analog MUX

### Features

- Fault and Overvoltage Protection
- All Channels Off When Power Off
- Latchup-Proof
- Fast Switching—$T_A$: 200 ns
- Break-Before-Make Switching
- Low On-Resistance: 180 Ω
- Low Power Consumption: 3 mW
- TTL and CMOS Compatible Inputs

### Benefits

- Improved Ruggedness
- Power Loss Protection
- Prevents Adjacent Channel Crosstalk
- Standard Logic Interface
- Superior Accuracy
- Fast Settling Time

### Applications

- Data Acquisition Systems
- Industrial Process Control Systems
- Avionics Test Equipment
- High-Rel Control Systems
- Telemetry

## Description

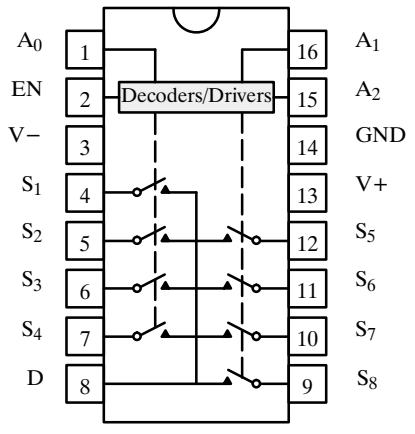
The DG458 and DG459 are 8-channel single-ended and 4-channel differential analog multiplexers, respectively, incorporating fault protection. A series n-p-n MOSFET structure provides device and signal-source protection in the event of power loss or overvoltages. Under fault conditions the multiplexer input (or output) appears as an open circuit and only a few nanoamperes of leakage current will flow. This protects not only the multiplexer and the circuitry following it, but also protects the sensors or signal sources which drive the multiplexer.

The DG458 and DG459 can withstand continuous overvoltage inputs up to ±35 V. All digital inputs have TTL compatible logic thresholds. Break-before-make operation prevents channel-to-channel interference.

The DG458 and DG459 are improved pin-compatible replacements for HI-508A/509A and MAX358/359 multiplexers.

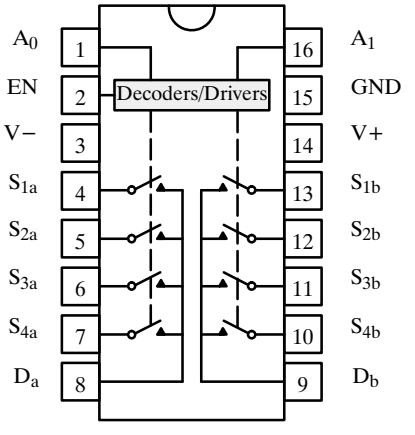
## Functional Block Diagrams and Pin Configurations

**DG458** Dual-In-Line




Top View

**DG459** Dual-In-Line




Top View

## Truth Tables and Ordering Information

**Truth Table — DG458**

| $A_2$ | $A_1$ | $A_0$ | EN | On Switch |
|---|---|---|---|---|
| X | X | X | 0 | None |
| 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 1 | 1 | 2 |
| 0 | 1 | 0 | 1 | 3 |
| 0 | 1 | 1 | 1 | 4 |
| 1 | 0 | 0 | 1 | 5 |
| 1 | 0 | 1 | 1 | 6 |
| 1 | 1 | 0 | 1 | 7 |
| 1 | 1 | 1 | 1 | 8 |

**Truth Table — DG459**

| $A_1$ | $A_0$ | EN | On Switch |
|---|---|---|---|
| X | X | 0 | None |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 1 | 2 |
| 1 | 0 | 1 | 3 |
| 1 | 1 | 1 | 4 |

Logic "0" = $V_{AL} \leq 0.8$ V
Logic "1" = $V_{AH} \geq 2.4$ V
X = Don't Care

**Ordering Information**

| Temp Range | Package | Part Number |
|---|---|---|
| −40 to 85°C | 16-Pin Plastic DIP | DG458DJ |
| | | DG459DJ |
| −55 to 125°C | 16-Pin CerDIP | DG458AK/883 |
| | | DG459AK/883 |
| | LCC-20 | DG458AZ/883 |
| | | DG459AZ/883 |

*Block Diagram and Pin Configuration not shown.

## Absolute Maximum Ratings

V+ to V− . . . . . 44 V
V+ to GND . . . . . 22 V
V− to GND . . . . . −25 V
$V_{EN}$, $V_A$ Digital Input . . . . . (V−) −4 V to (V+) +4 V
$V_S$, Analog Input Overvoltage with Power On . . . . . (V−) −20 V to (V+) +20 V
$V_S$, Analog Input Overvoltage with Power Off . . . . . −35 V to +35 V
Continuous Current, S or D . . . . . 20 mA
Peak Current, S or D (Pulsed at 1 ms, 10% Duty Cycle Max) . . . . . 40 mA

Storage Temperature (AK Suffix) . . . . . −65 to 150°C
(DJ Suffix) . . . . . −65 to 125°C
Power Dissipation (Package)[a]
16-Pin Plastic DIP[b] . . . . . 600 mW
16-Pin CerDIP[c] . . . . . 1000 mW
LCC-20[d] . . . . . 1000 mW

Notes:
a. All leads soldered or welded to PC board.
b. Derate 6.3 mW/°C above 25°C.
c. Derate 12 mW/°C above 75°C.
d. Derate 10 mW/°C above 75°C.

## Specifications[a]

| Parameter | Symbol | Test Conditions Unless Otherwise Specified<br>V+ = 15 V, V− = −15 V<br>$V_{AL}$ = 0.8 V, $V_{AH}$ = 2.4 V[f] | | Temp[b] | Typ[c] | A Suffix −55 to 125°C<br>Min[d] | A Suffix −55 to 125°C<br>Max[d] | D Suffix −40 to 85°C<br>Min[d] | D Suffix −40 to 85°C<br>Max[d] | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| **Analog Switch** | | | | | | | | | | |
| Analog Signal Range[g] | $V_{ANALOG}$ | | | Full | | −10 | 10 | −10 | 10 | V |
| Drain-Source On-Resistance | $r_{DS(on)}$ | $V_D$ = ±9.5 V, $I_S$ = −400 µA | | Room<br>Full | 0.45 | | 1.2<br>1.5 | | 1.5<br>1.8 | kΩ |
| | | $V_D$ = ±5 V, $I_S$ = −400 µA | | Room | 180 | | 400 | | 400 | Ω |
| $r_{DS(on)}$ Matching Between Channels[h] | $\Delta r_{DS(on)}$ | $V_D$ = 0 V, $I_S$ = −400 µA | | Room | 6 | | | | | % |
| Source Off Leakage Current | $I_{S(off)}$ | $V_{EN}$ = 0 V<br>$V_S$ = ±10 V, $V_D$ = ∓10 V | | Room<br>Full | 0.03 | −0.5<br>−50 | 0.5<br>50 | −1<br>−20 | 1<br>20 | nA |
| Drain Off Leakage Current | $I_{D(off)}$ | $V_{EN}$ = 0 V<br>$V_D$ = ±10 V<br>$V_S$ = ∓10 V | DG458 | Room<br>Full | 0.1 | −1<br>−200 | 1<br>200 | −1<br>−50 | 1<br>50 | |
| | | | DG459 | Room<br>Full | 0.1 | −1<br>−100 | 1<br>100 | −2<br>−25 | 2<br>25 | |
| Differential Off Drain Leakage Current | $I_{DIFF}$ | DG459 Only | | Room | | −50 | 50 | −20 | 20 | |
| Drain On Leakage Current | $I_{D(on)}$ | $V_S$ = $V_D$ = ±10 V | DG458 | Room<br>Full | 0.1 | −2<br>−200 | 2<br>200 | −5<br>−50 | 5<br>50 | |
| | | | DG459 | Room<br>Full | 0.05 | −2<br>−100 | 2<br>100 | −5<br>−25 | 5<br>25 | |
| **Fault** | | | | | | | | | | |
| Output Leakage Current (with Overvoltage) | $I_{D(off)}$ | $V_S$ = ±33 V, $V_D$ = 0 V<br>See Figure 1 | | Room | 0.02 | | | | | nA |
| Input Leakage Current (with Overvoltage) | $I_{S(off)}$ | $V_S$ = ±25 V, $V_D$ = ±10 V,<br>See Figure 1 | | Room | 0.005 | −5 | 5 | −10 | 10 | µA |
| Input Leakage Current (with Power Supplies Off) | | $V_S$ = ±25 V, $V_{SUPS}$ = 0 V<br>$V_D$ = $A_0$, $A_1$, $A_2$, EN = 0 V | | Room | 0.001 | −2 | 2 | −5 | 5 | |
| **Digital Control** | | | | | | | | | | |
| Input Low Threshold | $V_{AL}$ | | | Full | | | 0.8 | | 0.8 | V |
| Input Low Threshold | $V_{AL}$ | | | Full | | 2.4 | | 2.4 | | |
| Logic Input Control | $I_A$ | $V_A$ = 2.4 V or 0.8 V | | Full | | −1 | 1 | −1 | 1 | µA |
| **Dynamic Characteristics** | | | | | | | | | | |
| Transition Time | $t_A$ | See Figure 2 | | Room | 200 | | 500 | | 500 | ns |
| Break-Before-Make Time | $t_{OPEN}$ | See Figure 3 | | Room | 45 | 10 | | 10 | | |
| Enable Turn-On Time | $t_{ON(EN)}$ | See Figure 4 | | Room<br>Full | 140 | | 250<br>500 | | 250<br>500 | |
| Enable Turn-Off Time | $t_{OFF(EN)}$ | | | Room<br>Full | 50 | | 250<br>500 | | 250<br>500 | |
| Settling Time | $t_s$ | To 0.1 % | | Room | 0.5 | | | | | µs |
| | | To 0.01% | | Room | 1.5 | | | | | |
| Off Isolation | OIRR | $V_{EN}$ = 0 V, $R_L$ = 1 kΩ, $C_L$ = 15 pF<br>$V_S$ = 3 $V_{RMS}$, f = 100 kHz | | Room | 90 | | | | | dB |
| Logic Input Capacitance | $C_{in}$ | f = 1 MHz | | Room | 5 | | | | | pF |
| Source Off Capacitance | $C_{S(off)}$ | | | Room | 5 | | | | | |
| Drain Off Capacitance | $C_{D(off)}$ | | DG458 | Room | 15 | | | | | |
| | | | DG459 | Room | 10 | | | | | |
| Drain On Capacitance | $C_{D(on)}$ | | DG458 | Room | 40 | | | | | |
| | | | DG459 | Room | 35 | | | | | |

## Specifications[a]

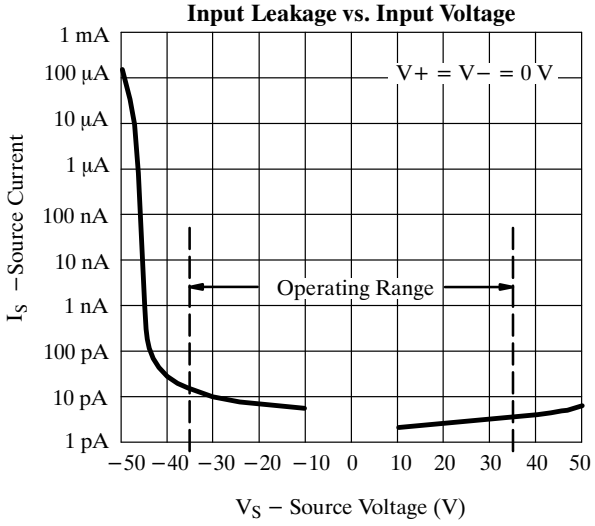
| Parameter | Symbol | Test Conditions Unless Otherwise Specified<br>V+ = 15 V, V− = −15 V<br>$V_{AL}$ = 0.8 V, $V_{AH}$ = 2.4 V[f] | Temp[b] | Typ[c] | A Suffix −55 to 125°C | | D Suffix −40 to 85°C | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | Min[d] | Max[d] | Min[d] | Max[d] | |
| **Power Supplies** | | | | | | | | | |
| Positive Supply Current | I+ | $V_{EN}$ = 5.0 or 0 V, $V_A$ = 0 V | Room<br>Full | 0.05 | | 0.1<br>0.2 | | 0.1<br>0.2 | mA |
| Negative Supply Current | I− | | Room<br>Full | −0.01 | −0.1<br>−0.2 | | −0.1<br>−0.2 | | |
| Power Supply Range for Continuous Operation | | | Room | | ±4.5 | ±18 | ±4.5 | ±18 | V |

Notes:
a. Refer to PROCESS OPTION FLOWCHART (Section 5 of the 1994 Data Book or FaxBack number 7103).
b. Room = 25°C, Full = as determined by the operating temperature suffix.
c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
d. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
e. Guaranteed by design, not subject to production test.
f. $V_{IN}$ = input voltage to perform proper function.
g. When the analog signal exceeds the +13.5 V or −12 V, $r_{DS(on)}$ starts to rise until only leakage currents flow.
h.

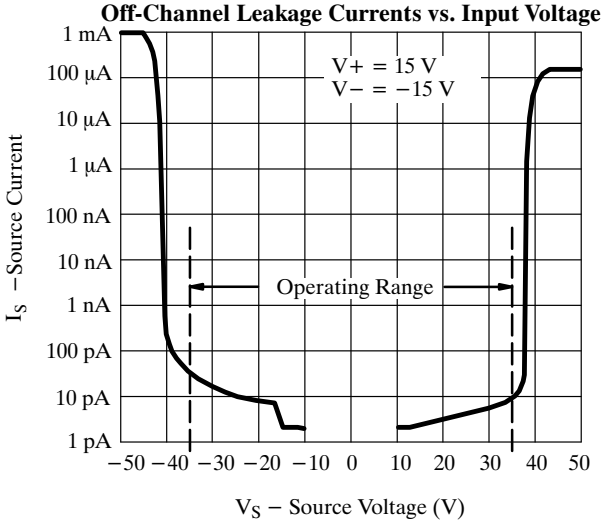
$$\Delta r_{DS(on)} = \left( \frac{r_{DS(on)}\ \text{MAX} - r_{DS(on)}\ \text{MIN}}{r_{DS(on)}\ \text{AVE}} \right) \text{x } 100\%$$

## Typical Characteristics

**Input Leakage vs. Input Voltage**

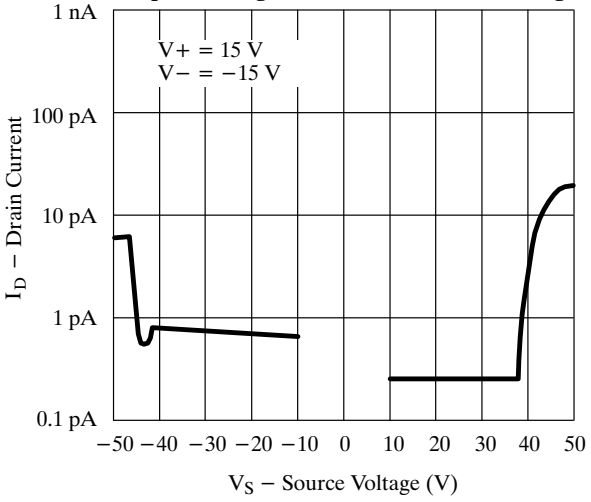



**Off-Channel Leakage Currents vs. Input Voltage**

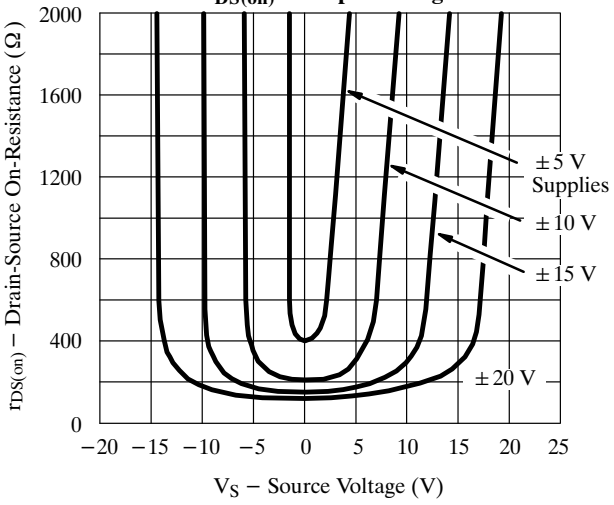


## Typical Characteristics (Cont'd)

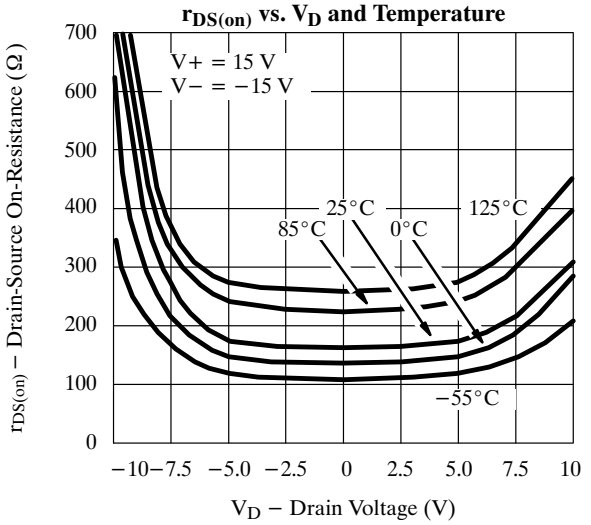
**Output Leakage vs. Off-Channel Overvoltage**



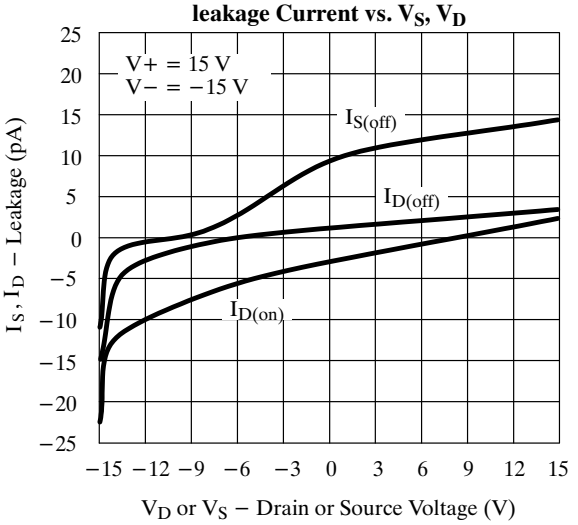

**$r_{DS(on)}$ vs. Input Voltage**



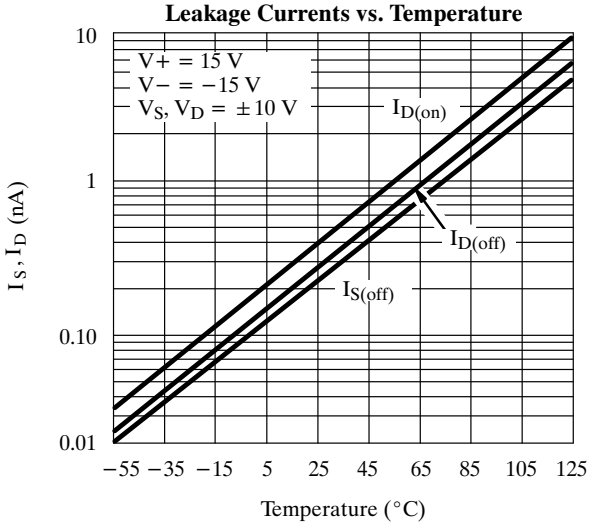

**$r_{DS(on)}$ vs. $V_D$ and Temperature**



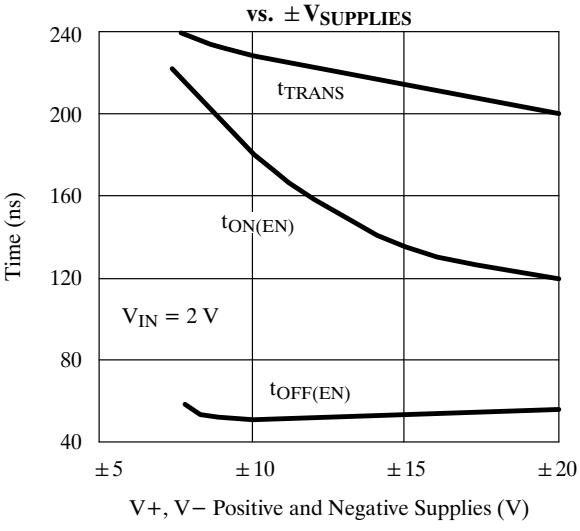

**leakage Current vs. $V_S$, $V_D$**




**Leakage Currents vs. Temperature**

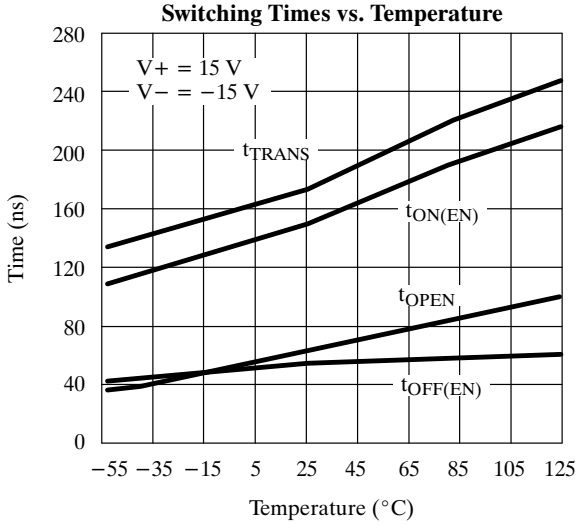



**Switching Times ($t_{TRANS}$, $t_{ON}$, $t_{OFF}$) vs. $\pm V_{SUPPLIES}$**

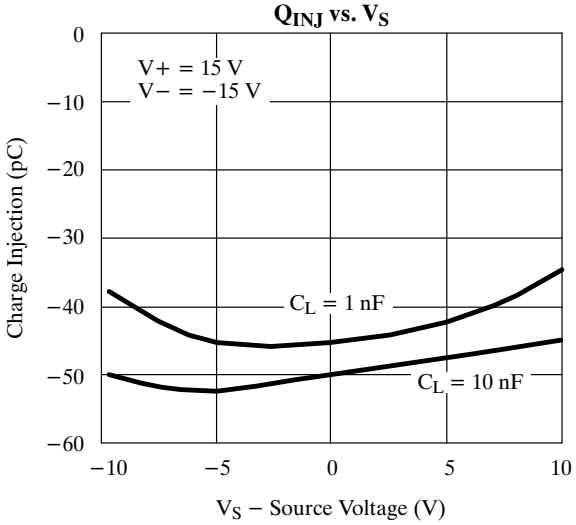


## Typical Characteristics (Cont'd)

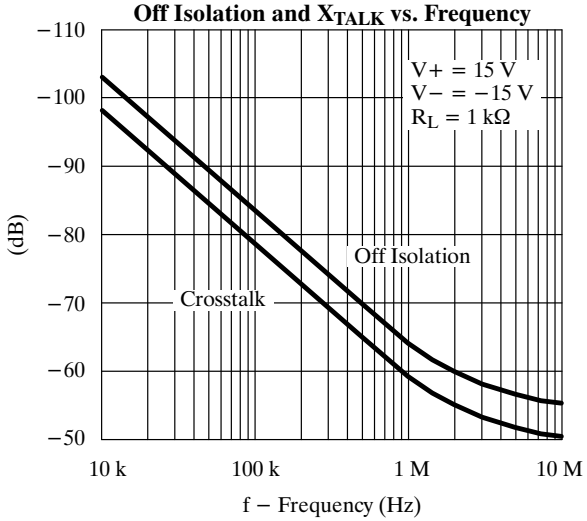
**Switching Times vs. Temperature**



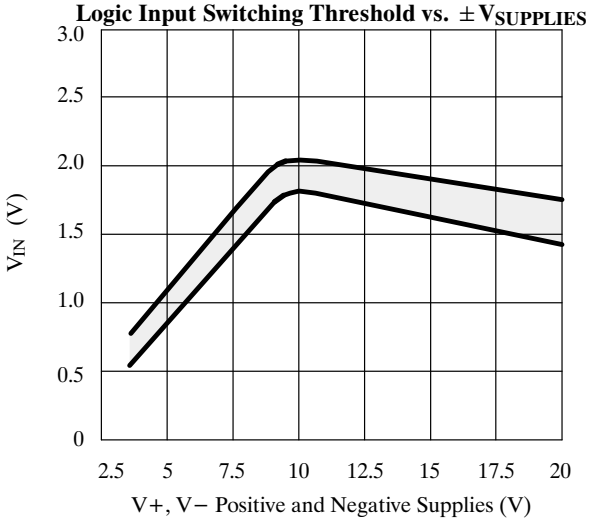

**$Q_{INJ}$ vs. $V_S$**




**Off Isolation and $X_{TALK}$ vs. Frequency**




**Logic Input Switching Threshold vs. $\pm V_{SUPPLIES}$**



## Schematic Diagram (Typical Channel)

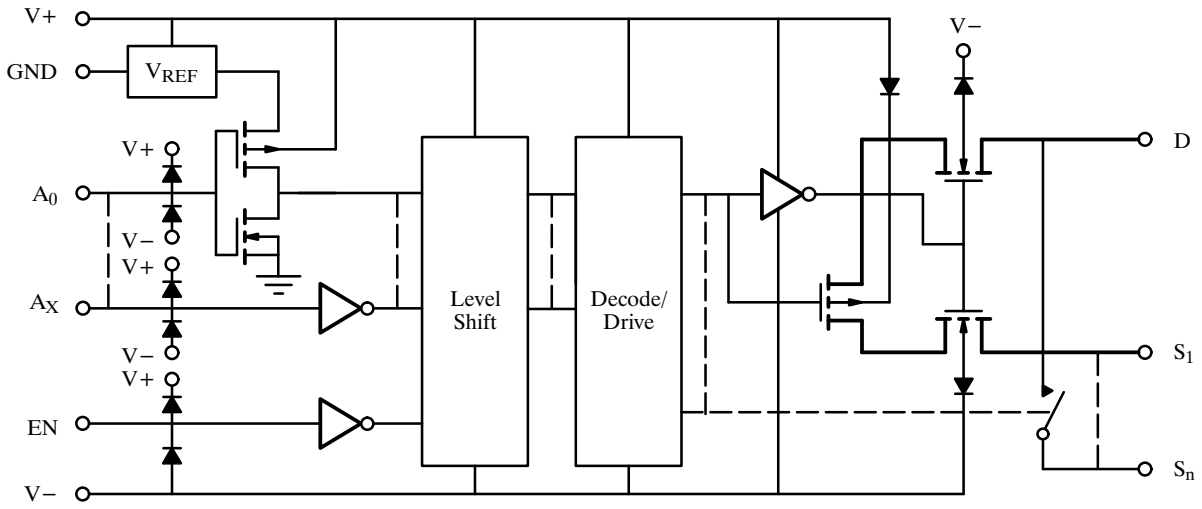



**Figure 1.**

## Test Circuits

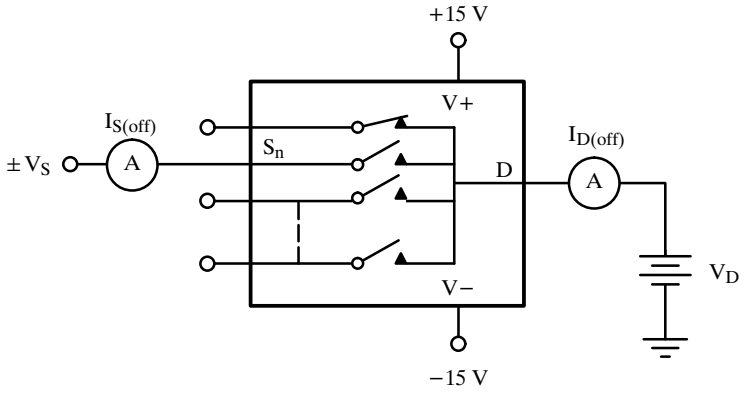
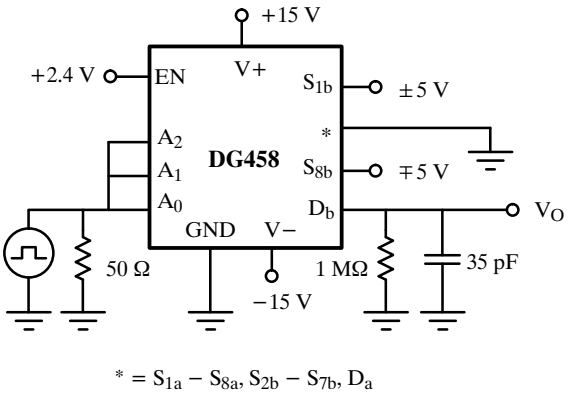



**Figure 2.** Analog Input Overvoltage

## Test Circuits (Cont'd)



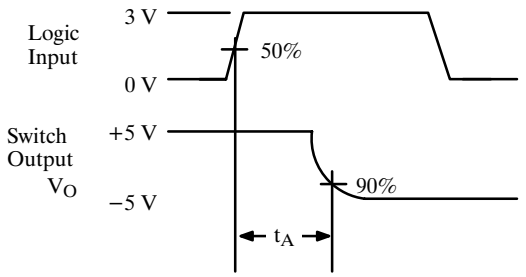
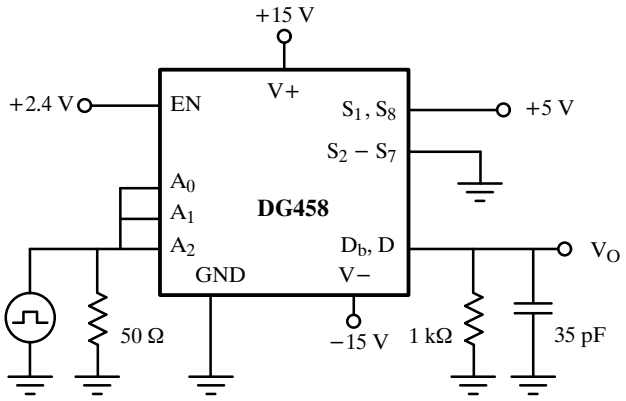




**Figure 3.** Transition Time



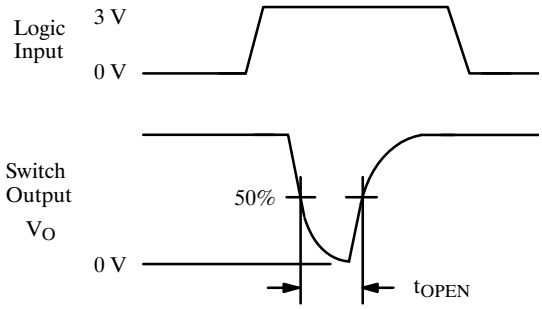
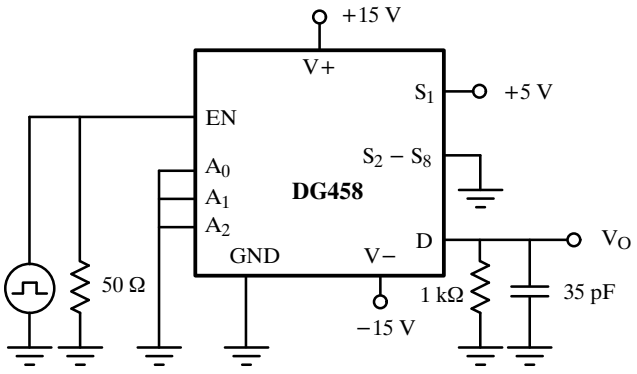




**Figure 4.** Break-Before-Make Time



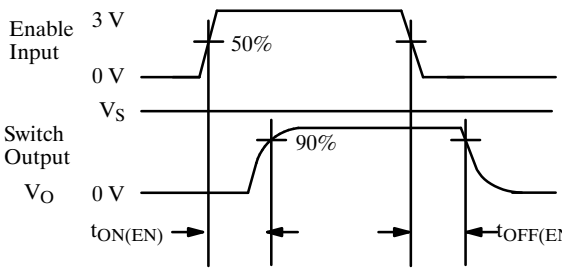



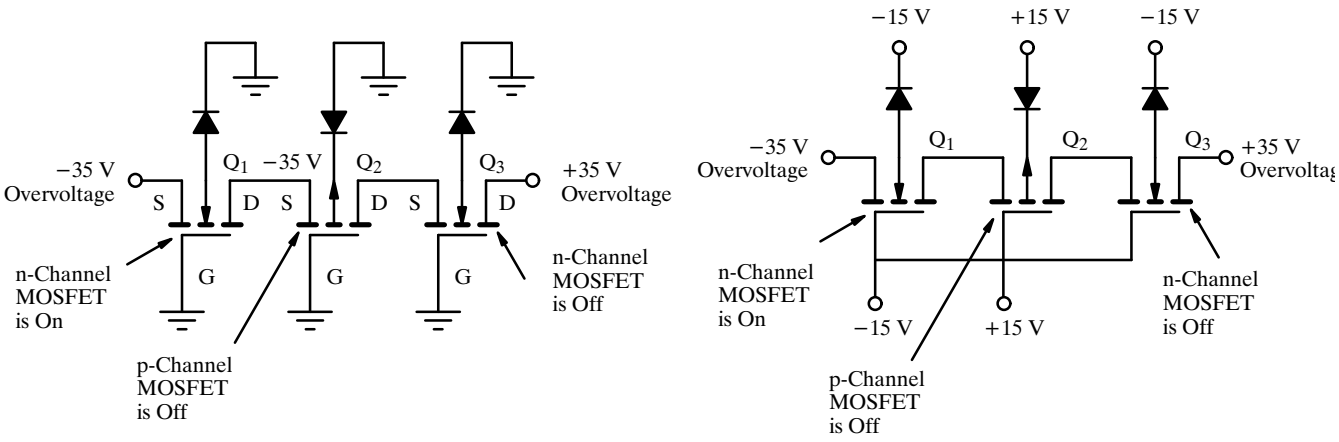

**Figure 5.** Enable Delay

## Detailed Description

The Siliconix DG458 and DG459 multiplexers are fully fault- and overvoltage-protected for continuous input voltages up to ±35 V whether or not voltage is applied to the power supply pins (V+, V−). These multiplexers are built on a high-voltage junction-isolated silicon-gate CMOS process. Two n-channel and one p-channel MOSFETs are connected in series to form each channel (Figure 17).

Within the normal analog signal range (±10 V), the $r_{DS(on)}$ variation as a function of analog signal voltage is comparable to that of the classic parallel N-MOS and P-MOS switches.

When the analog signal approaches or exceeds either supply rail, even for an on-channel, one of the three series MOSFETs gets cut-off, providing inherent protection against overvoltages even if the multiplexer power supply voltages are lost. This protection is good up to the breakdown voltage of the respective series MOSFETs. Under fault conditions only sub microamp leakage currents can flow in or out of the multiplexer. This not only provides protection for the multiplexer and succeeding circuitry, but it allows normal, undisturbed operation of all other channels. Additionally, in case of power loss to the multiplexer, the loading caused on the transducers and signal sources is insignificant, therefore redundant multiplexers can be used on critical applications such as telemetry and avionics.




**(a) Overvoltage with Multiplexer Power Off**

**(b) Overvoltage with Multiplexer Power On**

**Figure 6.** Overvoltage Protection